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2018-2019 M.TECH VLSI IEEE TITLES

S.No	TITLES	Year
	VLSI	
1	Approximate Quaternary Addition with the Fast Carry Chains of FPGAs	2018
2	A Low-Power Configurable Adder for Approximate Applications	2018
3	A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design	2018
4	A Low-Power Yet High-Speed Configurable Adder for Approximate Computing	2018
5	A Simple Yet Efficient Accuracy- Configurable Adder Design	2018
6	Adaptive Approximation in Arithmetic Circuits: A Low-Power Unsigned Divider Design	2018

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7	Approximate Hybrid High Radix Encoding for Energy-Efficient Inexact Multipliers	2018
8	A Cost-Effective Self-Healing Approach for Reliable Hardware Systems	2018
9	Approximate Sum-of-Products Designs Based on Distributed Arithmetic	2018
10	Design and Evaluation of Approximate Logarithmic Multipliers for Low Power Error-Tolerant Applications	2018
11	Design, Evaluation and Application of Approximate High-Radix Dividers	2018
12	Efficient Fixed/Floating-Point Merged Mixed-Precision Multiply-Accumulate Unit for Deep Learning Processors	2018
13	Enhancing Fundamental Energy Limits of Field-Coupled Nano computing Circuits	2018
14	Exploration of Approximate Multipliers Design	2018

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	Space using Carry Propagation Free Compressors	
15	Inexact Arithmetic Circuits for Energy Efficient IOT Sensors Data Processing	2018
16	Low-Power Addition With Borrow-Save Adders Under Threshold Voltage Variability	2018
17	Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system	2018
18	On the Difficulty of Inserting Trojans in Reversible Computing Architectures	2018
19	Optimizing Power-Accuracy trade-off in Approximate Adders	2018
20	Power Efficient Approximate Booth Multiplier	2018
21	Reducing the Hardware Complexity of a Parallel Prefix Adder	2018
22	Systematic Design of an Approximate Adder: The Optimized Lower Part Constant-OR Adder	2018

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2	A Bit-Plane Decomposition Matrix-Based VLSI Integer Transform Architecture for HEVC	2017
3	An Efficient $O(N)$ Comparison-Free Sorting Algorithm	2017
4	An Improved DCM-Based Tunable True Random Number Generator for Xilinx FPGA	2017
5	Clock-Gating of Streaming Applications for Energy Efficient Implementations on FPGAs	2017
6	Design of Efficient BCD Adders in Quantum-Dot Cellular Automata	2017
7	Design of Efficient Multiplierless Modified Cosine-Based Comb Decimation Filters: Analysis and Implementation	2017
8	Design of Power and Area Efficient Approximate Multipliers	2017
9	Efficient Hardware Implementation of Probabilistic Gradient Descent Bit-Flipping	2017
10	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations	2017

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13	Overloaded CDMA Crossbar for Network-On-Chip	2017
14	Probabilistic Error Modeling for Approximate Adders	2017
15	Probability-Driven Multibit Flip-Flop Integration With Clock Gating	2017
16	Reliable Low-Latency Viterbi Algorithm Architectures Benchmarked on ASIC and FPGA	2017
17	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing	2017

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21	A General Digit-Serial Architecture for Montgomery Modular Multiplication	2017
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27	DLAU: A Scalable Deep Learning Accelerator Unit on FPGA	2017
28	Energy-Efficient VLSI Realization of Binary64 Division With Redundant Number Systems	2017
29	High-Throughput and Energy-Efficient Belief Propagation Polar Code Decoder	2017
30	LLR-Based Successive-Cancellation List Decoder for Polar Codes With Multi bit Decision	2017

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32	On the VLSI Energy Complexity of LDPC Decoder Circuits	2017
33	Reconfigurable Constant Multiplication for FPGAs	2017
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