

# CEGON TECHNOLOGIES

S.NO	PROJECT NAME	YEAR
1	A 4096-Point Radix-4 Memory-Based FFT Using DSP Slices	2017
2	A Bit-Plane Decomposition Matrix-Based VLSI Integer Transform Architecture for HEVC	2017
3	An Efficient $O(N)$ Comparison-Free Sorting Algorithm	2017
4	An Improved DCM-Based Tunable True Random Number Generator for Xilinx FPGA	2017
5	Clock-Gating of Streaming Applications for Energy Efficient Implementations on FPGAs	2017
6	Design of Efficient BCD Adders in Quantum-Dot Cellular Automata	2017
7	Design of Efficient Multiplierless Modified Cosine-Based Comb Decimation Filters: Analysis and Implementation	2017
8	Design of Power and Area Efficient Approximate Multipliers	2017
9	Efficient Hardware Implementation of Probabilistic Gradient Descent Bit-Flipping	2017
10	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations	2017
11	Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction	2017
12	LFSR-Based Generation of Multicycle Tests	2017
13	Overloaded CDMA Crossbar for Network-On-Chip	2017

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*\*Rupai Midde Upstair , Trunk Road , Kavali.\**

*\*Ph\*\*: 7396555247*

**CEGONTECHNOLOGIES@GMAIL.COM**

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14	Probabilistic Error Modeling for Approximate Adders	2017
15	Probability-Driven Multibit Flip-Flop Integration With Clock Gating	2017
16	Reliable Low-Latency Viterbi Algorithm Architectures Benchmarked on ASIC and FPGA	2017
17	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing	2017
18	Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST	2017
19	Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication	2017
20	Weighted Partitioning for Fast Multiplierless Multiple-Constant Convolution Circuit	2017
21	A General Digit-Serial Architecture for Montgomery Modular Multiplication	2017
22	A Memory-Based FFT Processor Design With Generalized Efficient Conflict-Free Address Schemes	2017

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23	A Structured Visual Approach to GALS Modelling and Verification of Communication Circuits	2017
24	Area-Efficient Architecture for Dual-Mode Double Precision Floating Point Division	2017
25	Area-Time Efficient Architecture of FFT-Based Montgomery Multiplication	2017
26	Digit-Level Serial-In Parallel-Out Multiplier Using Redundant Representation for a Class of Finite Fields	2017
27	DLAU: A Scalable Deep Learning Accelerator Unit on FPGA	2017
28	Energy-Efficient VLSI Realization of Binary64 Division With Redundant Number Systems	2017
29	High-Throughput and Energy-Efficient Belief Propagation Polar Code Decoder	2017
30	LLR-Based Successive-Cancellation List Decoder for Polar Codes With Multi bit Decision	2017
31	Low-Latency, Low-Area, and Scalable Systolic-Like Modular Multipliers for GF(2 <sup>m</sup> ) Based on Irreducible All-One Polynomials	2017

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32	On the VLSI Energy Complexity of LDPC Decoder Circuits	2017
33	Reconfigurable Constant Multiplication for FPGAs	2017
34	An Improved Design of a Reversible Fault Tolerant LUT-Based FPGA	2017
35	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	2017

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